Description

This Power MOSFET is produced using Hua semiconductor's advanced SGT MOSFET technology. This product has been designed and will qualified to AEC Q101 standard for use in high performance automotive applications.

Features

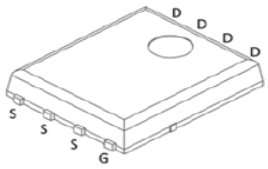
- RDS(on) = 3.3 mΩ (max.) @ VGS = 10V, ID = 20A
- Low FOM RDS(on)*QG
- Low Reverse Recovery Charge, Qrr
- Q101 compliant
- RoHS Compliant

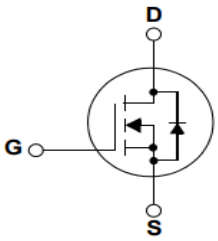
Applications

- Switching power supplies
- Power switches

Package and Ordering

Part Number	Goods picture
Package	DFN5060
Mark	90N04G
Packing	Tape & Reel
Quantity	2500





Maximum Ratings T_J =25 °C unless otherwise noted

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		40	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Continuous Drain Current-$R_{\theta JC}$	T_C = 25°C	40	A
I_{DM}	Pulsed Drain Current	T_C = 25°C	332	A
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1)	T_C = 25°C	50	W
		T_C = 100°C	25	
T_L	Lead Temperature for Soldering Purposes-10 sec		260	°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	45	°C/W

Electrical Characteristics

Static characteristics T_J =25 °C unless otherwise noted

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
B_{VDSS}	Drain to Source Breakdown Voltage	ID = 250 μA, VGS = 0 V	40	-	-	V
ΔBVDSS / ΔTJ	Breakdown Voltage Temperature Coefficient	ID = 250 μA, Referenced to 25°C	-	25	-	mV/°C
IDSS	Drain to Source Leakage	VDS = 40 V, VGS = 0 V Tj=25°C	-	-	1	μA
		VDS = 40 V, VGS = 0 V Tj=125°C	-	-	100	μA
IGSS	Gate to Source Leakage	VGS = ±20 V, VDS = 0 V	-	-	±100	nA
$VGS_{(th)}$	Gate Threshold Voltage	VGS = VDS, ID = 250 μA	2.4	-	3.4	V
$RDS_{(on)}$	Static Drain to Source On Resistance	Vgs=10V, ID=20A Tj=25°C	-	3.3	4.3	mΩ
R_g	Gate Resistance	f = 1 MHz	-	2.8	-	Ω
gfs	Forward Transconductance	Vds=5V, ID=20A	-	50	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 20 V, VGS = 0 V,f = 1 MHz	-	1330	-	pF
C_{oss}	Output Capacitance		-	760	-	pF
C_{rss}	Reverse Transfer Capacitance		-	55	-	pF
Qg	Total Gate Charge	VGS=10V,VDS=20V,ID=20A	-	18	-	nC
Q_{gs}	Gate to Source Charge		-	5	-	nC
Q_{gd}	Gate to Drain (Miller) Charge		-	3.4	-	nC

Drain-Source Diode Characteristics

V_{SD}	Drain to Source Diode Forward Voltage	Vgs=0V, ID=20A Tj=25°C	-	0.8	1.2	V
T_{rr}	Reverse Recovery Time	DI/DT=100A/us,ID=20A	-	45	-	nS
Q_{rr}	Reverse Recovery Charge		-	35	-	nC

Notes:

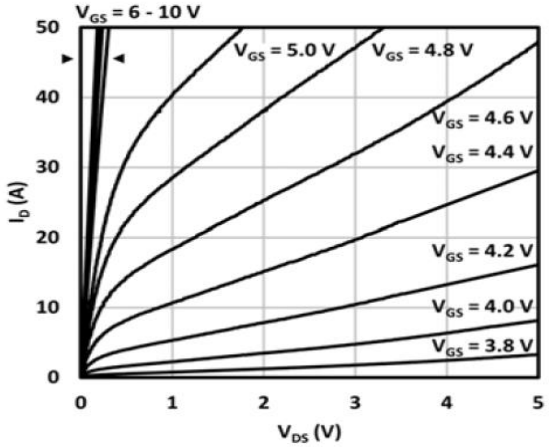
1. they are not constants value, your application eenvironment will effect them.

2. RθJA is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. RθJC is guaranteed by design while RθJA is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in2 pad of 2oz copper.

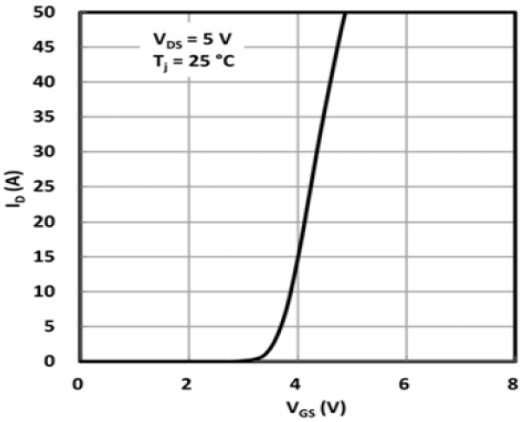
3.it is limited by $T_{j\ max}$.

Typical Performance Characteristics

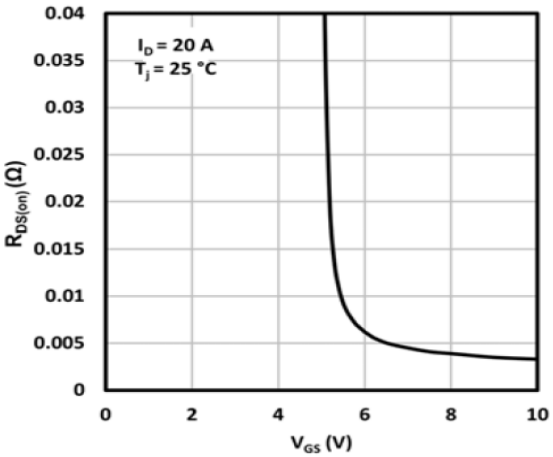
1. Output characteristics



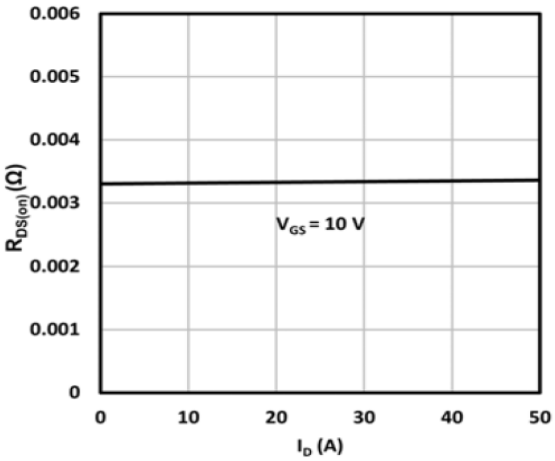
2. Transfer characteristics



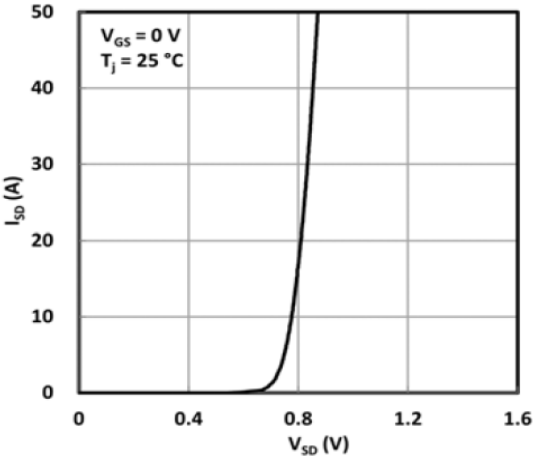
3. On-resistance vs. gate voltage



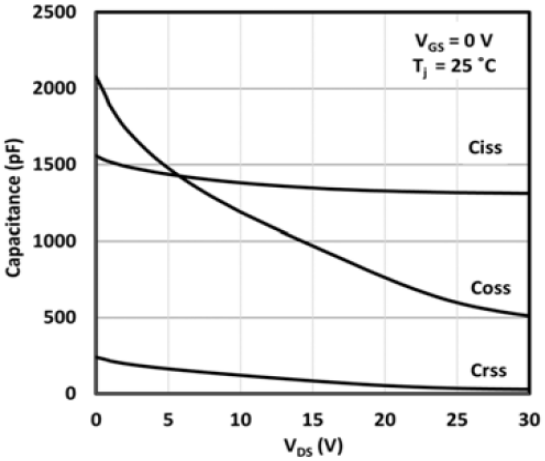
4. On-resistance vs. drain current



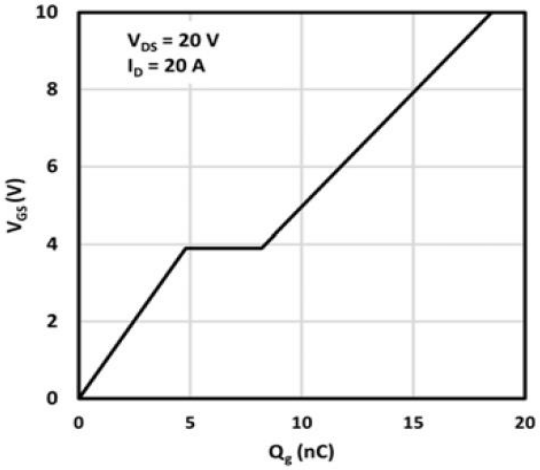
5. diode forward characteristics



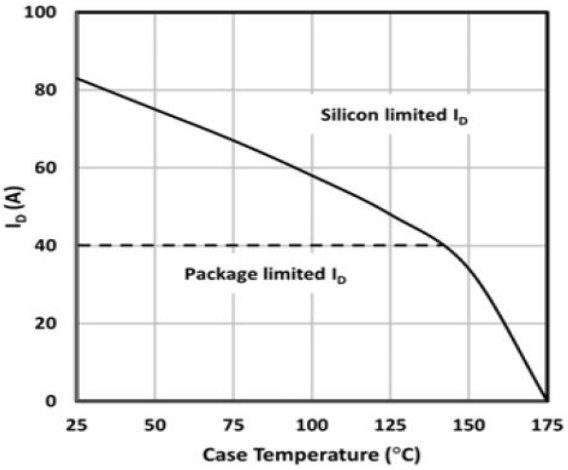
6. Capacitance



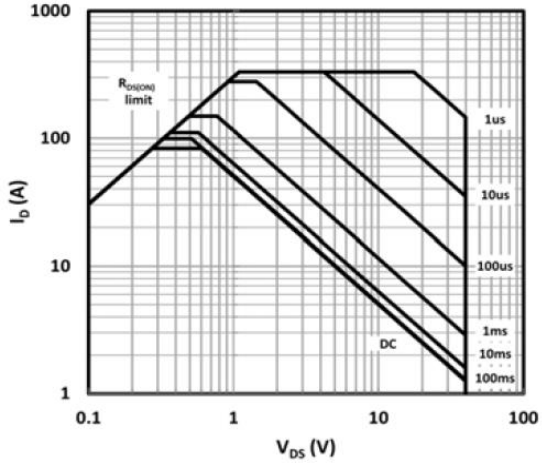
6. gate charge



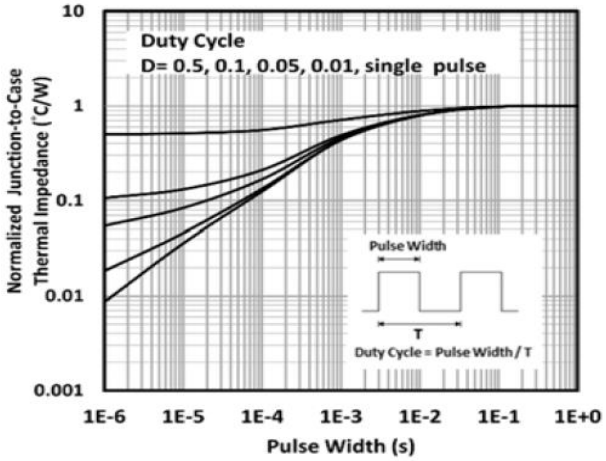
7. Maximum drain current



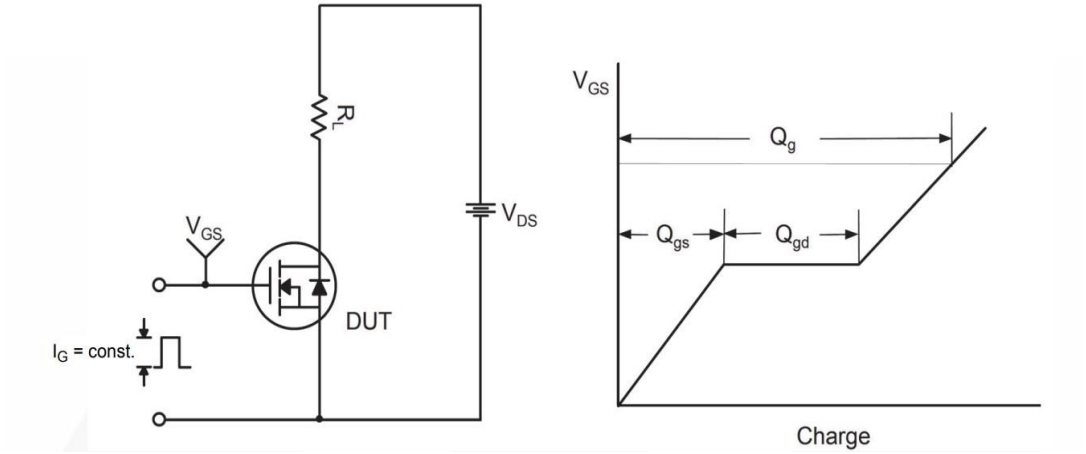
8. Safe operating area



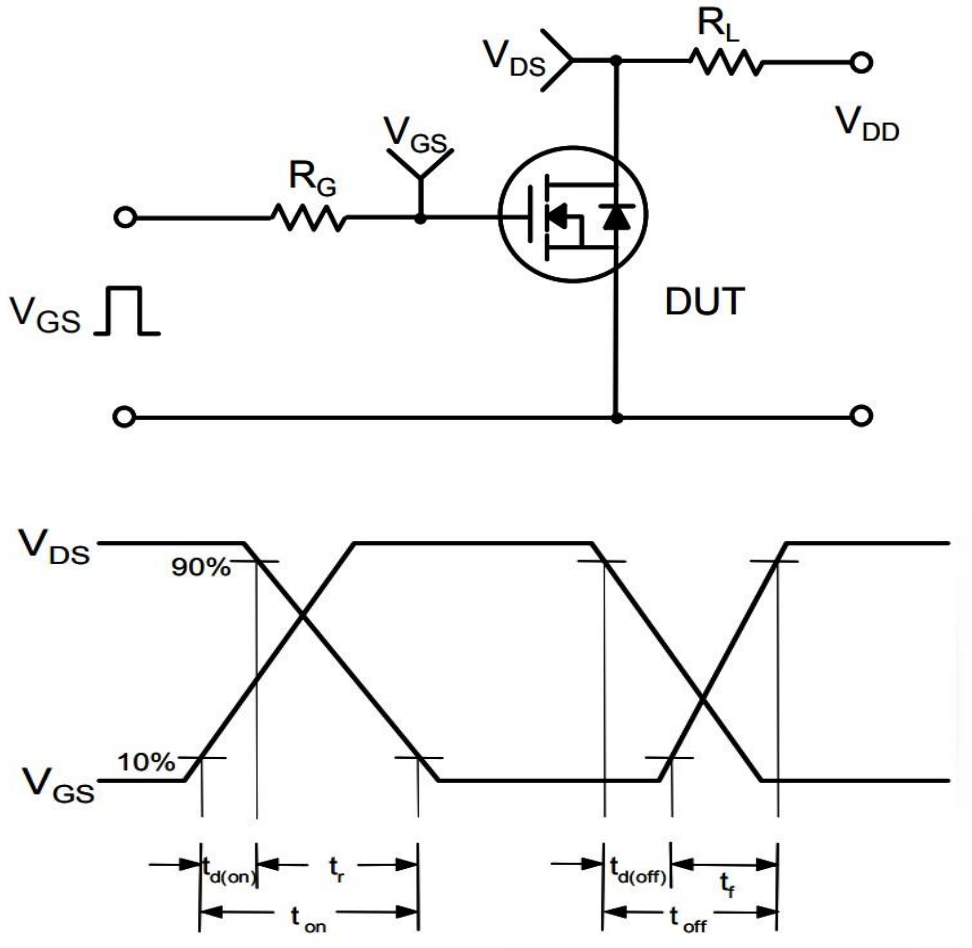
9. thermal impedance



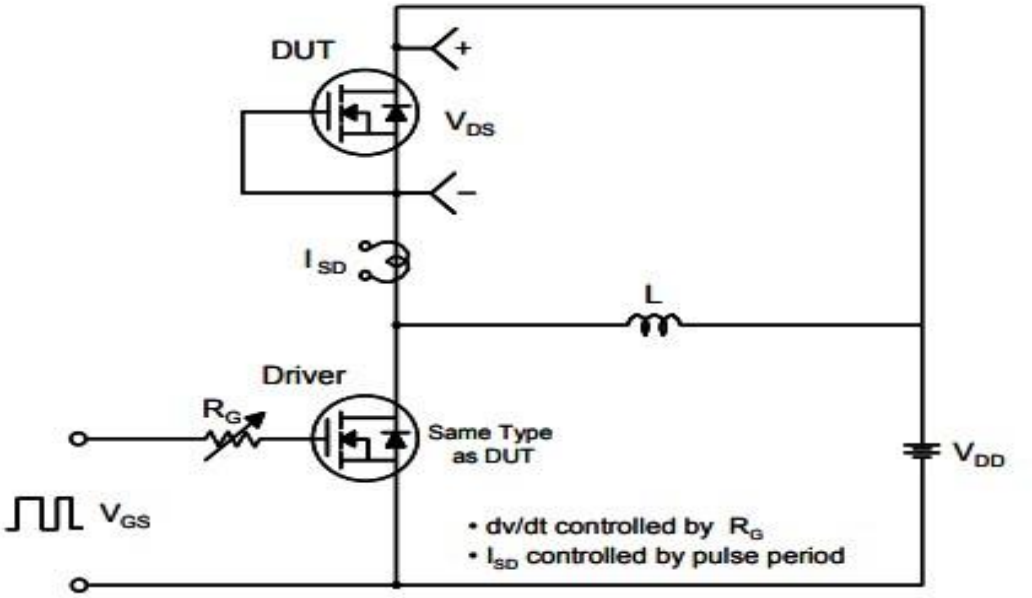
12. Gate Charge Test Circuit & Waveform

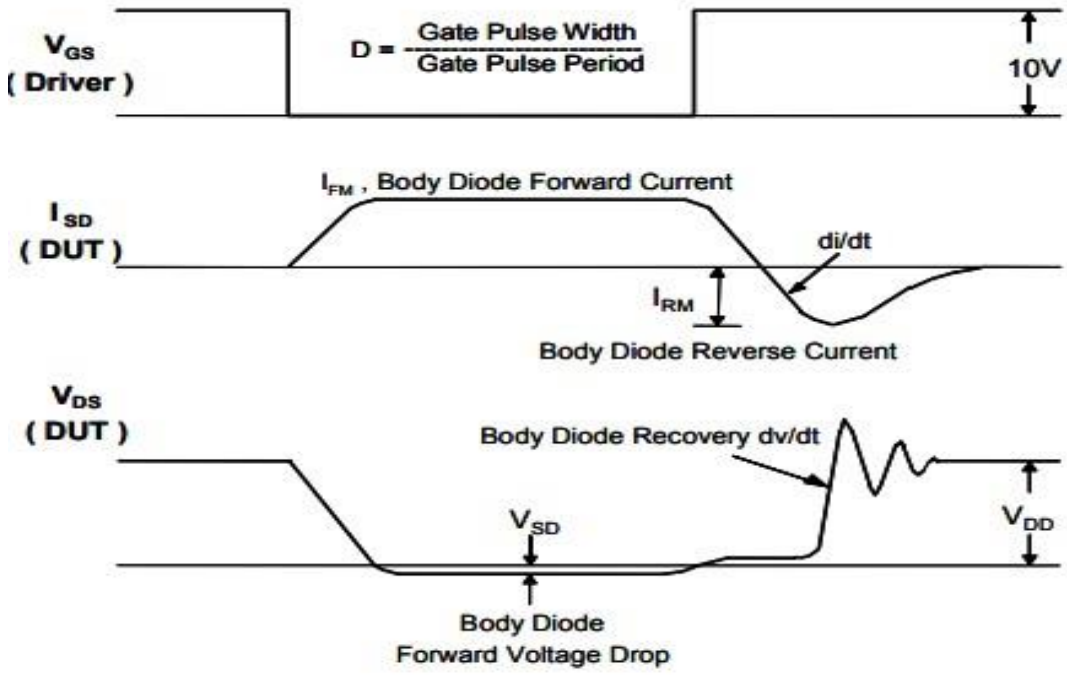


13. Switching Test Circuit & Waveform

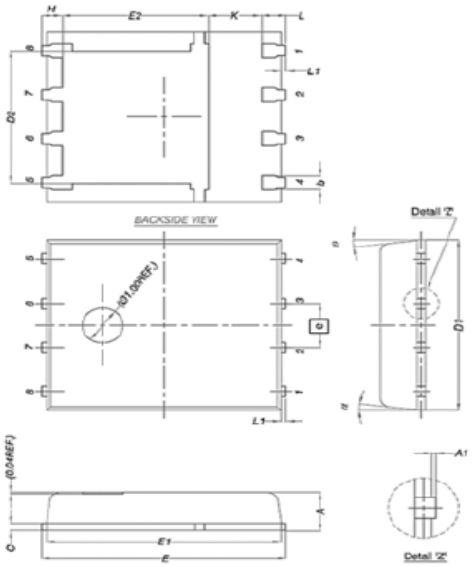


14. Peak Diode Recovery dv/dt Test Circuit & Waveforms





DFN5060 Package Case Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°